

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Akhil K. Garlapati et al.

Title: VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA  
EFFECT OF A CMOS BIPOLAR TRANSISTOR

Application No.: 10/813,837

Filed: March 31, 2004

Examiner: Rajnikant B. Patel

Group Art Unit: 2838

Atty. Docket No.: 026-0044

Confirmation No.: 6047

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August 2, 2007

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

### **RESPONSE TO NON-FINAL OFFICE ACTION**

This paper is responsive to the Non-Final Office Action mailed on May 7, 2007. In light of the Amendments and/or Remarks herein, further consideration is requested.

Any fees required by this paper are being provided as directed in an electronic submission of this paper or in a transmittal letter accompanying this paper. However, the Commissioner is hereby authorized to charge any deficiency in fees required by this paper and any additional fees under 37 C.F.R. § 1.16 or 1.17 which may be required during the pendency of this application, and to similarly credit any overpayment, to Deposit Account 50-0631.